Design and implementation of FFT algorithm for MB-OFDM with parallel architecture

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Abstract

Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. OFDM timing synchronization accuracy is evaluated for each system at different signal-to-noise ratios. This can be used in digital television, audio broadcasting, DSL Broadband internet access, wireless networks and 4G mobile communications. For OFDM design the existing system consists of radix-2 Based FFT algorithm architecture that can be capable of working in Single band multi carrier frequency, in order to change that architecture we prefer a new algorithm with new radix architecture. The proposed method is to develop a mixed Radix Based FFT Algorithm for the analysis of Multiband OFDM and their FPGA parameters calculation, in order to reduce the complexity for the efficient operation of MB- OFDM. Mixed radix FFT algorithm and the SFO, CFO, Channel equalizer blocks which can provide an efficient operation for OFDM system. SFO and CFO blocks are used to improve the performance of the system.

KeyWords:*Correlation, IEEE802.16 standards, Orthogonal frequency division multiplexing(OFDM), Multiplierless structure, Radix-2FFT, Mixed Radix FFT, CFO,SFO.*

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1.INTRODUCTION

orthogonal frequency division multiplexing (OFDM) is a technique for encoding digital data on multiple carrier frequencies. OFDM is an effective modulation technique for both wired and wireless communication systems. It has an spectral efficiency and Robustness to multipath fading. OFDM is specifically used for multiple applications in high bitrate wireless transmission system such as wireless Local area network (802.11) and Metropolitan area network(802.16d).OFDM is more sensitive to receiver synchronization. Frequency offset which causes an inter-subcarrier interference and errors in timing synchronization can lead to inter-symbol-interference.so it creates critical synchronization for OFDM systems. To improve the synchronization accuracy for cyclic prefix method were introduced to determine the frequency offset and symbol timing offset (STO).All OFDM frames are begin with preamble symbols, which can be used to estimate the frequency offset. It focus on the characteristics of preamble symbols with two identical halves, using autocorrelation of the received signal, which can be computed at low cost and relatively robust to frequency offset. The modified timing metrics based on the autocorrelation and the characteristics of preamble symbol to reduce the ambiguity of plateau and determine the starting of frame. The autocorrelation operation is sensitive to Additive White Gaussian Noise(AWGN) and frequency selectivity. An accurate synchronization is based on preamble symbols specified for IEEE 802.16d of computation

process like in, autocorrelation of coarse symbol timing offset (STO) and fractional carrier frequency offset(CFO) to estimate an reliable frequency synchronization and reduce cost. But cross correlation for fine STO, integer CFO to perform between received samples and known preamble.. Highly parallel architecture are suitable for implementing the OFDM receivers. Accuracy of cross correlation algorithms are better compare than autocorrelation, but cross correlation has an hardware cost is high. . So make an modified approach for cross correlation to reduce hardware cost compare the classical approach. The new cross correlation is five times complex to implement compare than autocorrelation. The multiplier based correlator are require more power and hardware cost is hike. So the replacement of multiplier based structure to multiplierless structure with the help of shift add and multiplexer operations to achieve an same synchronization accuracy at radix2 FFT structure.

2 MB-OFDM PHY BASEBAND MODEM DESIGN OVERVIEW

Fig. 1 shows an overall architecture of MB-OFDM baseband modem that supports both transmission (TX) and reception (RX). MB-OFDM protocol standard was designed to process eight complex numbers of Transceiver signals at one time with 8-way parallel data paths. The baseband modem is created for various components for incoming data and deliver into their results. An 8-bit fixed-point representation are passed through input and output ports for complex numbers in each component. The preamble ROM which transmits an complex numbers of preamble sequences and packet synchronizer detects a received packet, the CFO compensator which estimates and compensates for the packet on TX side. The fast Fourier transform (FFT) module is shared for transceiver and it has a 128-point complex FFT ,which provides the throughput of 8 samples/cycle. The Proposed FFT module has an mixed combination of radix-2 and radix4 units. The

subcarrier(de)mappers are in charge of mapping a complex number to a corresponding subcarrier are processed in reverse direction.

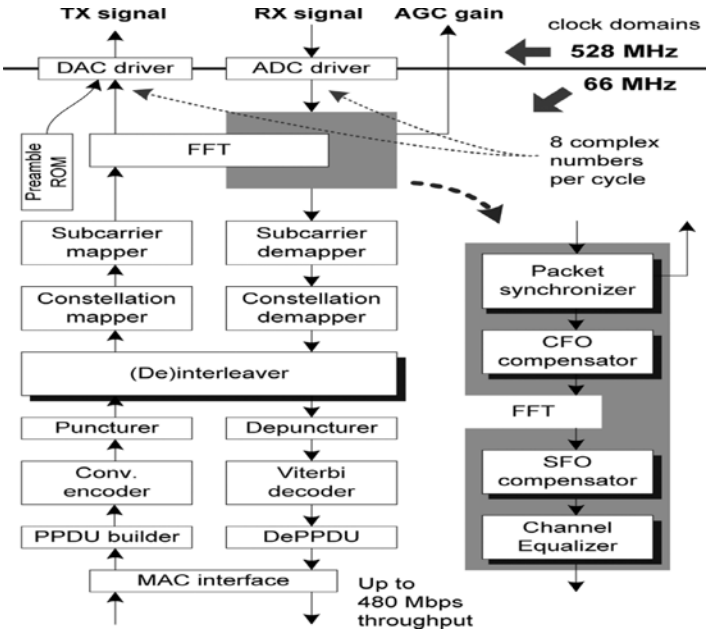


Fig 1 Overall architecture of Multiband OFDM

The constellation mapper which converts coded bits into complex numbers using the rules of quadrature phase-shift keying (QPSK) and dual-carrier modulation (DCM). The (de)interleaver randomly chooses the coded bit sequences (interleaving in TX) and recovers the original sequences (DE interleaving in RX) for improving decoding performance even in the presence of errors. The puncture rejects some coded bits in order to support different code rates with one convolutional encoder. The depuncturer which replace dummy bits for the rejected bits.

3 MB-OFDM PHY BASEBAND MODEM DESIGN OPTIMIZATION

This section provides detailed descriptions of (de)interleaver, packet synchronizer, CFO compensator, SFO compensator, and channel equalizer.

3.1 (De)Interleaver:

Interleaver systems performs step by step process like symbol interleaving, tone interleaving and cycle shift. This approach requires much chip resource and storage between sub process. The interleaver process has an long latency. So resolve this problem we use an mixed radix system(MRS). MRS process to provide an powerful interleaver structure for MB-OFDM system. MB-OFDM defines two constellations like QPSK and DCM modulations. The QPSK spreads data into several subcarriers and the DCM requires data reordering. The spreading and reordering processes involve non-trivial amount of buffer storages and also latency.

3.2 Packet Synchronizer:

Packet synchronizer has an the correlation function as auto correlation and cross correlation. The autocorrelation which carries the correlation between received signals and time instance to each other. While the cross correlation has an preamble pattern. Unfortunately auto correlation is not fit for the MB-OFDM system, So we preferred an cross correlation technique. The sampling frequency offset(SFO) compensator compensatesfor a sampling frequency offset with respect to the packet TX side and a channel equalizer mitigates signal distortions caused by each subcarrier channel.

$$C = \sum_{n=0}^{127} In(n).REF(n). \quad (1)$$

$$p = \sum_{n=0}^{127} |In(n)|^2 \quad (2)$$

Detect if , $|C|^2 > K.P$; K=15 (3)

The correlation can be implemented with adder instead of multipliers for,

$$R^+ = \{n = 0 \le n \le 127 \text{ and } REF(n) \ge 0\} \quad (4)$$

$$R^- = \{n: 0 \le n \le 127 \text{ and } REF(n) < 0\} \quad (5)$$

$$C = \rangle \quad In(n) - \sum_{n \in R_-}^{u} In(n) \quad (6)$$

4 PROPOSED SYSTEM

The downlink preamble in IEEE 802.16d contains two consecutive OFDM symbols, as shown in Fig 2(a). The short symbol consists of four identical 64-sample fragments in time, preceded by a Cyclic Prefix(CP). This is followed by the long symbol which contains two repetitions of a 128-sample fragment and a CP.. Therefore, the correlators are designed to compute cross-correlation with 64 constant coefficients. The output is the sum of 64 coefficient products, with each smaller than unity. Fig 2(b) which shows an basic structure of multiply-adder.That structure which shows an pipline sequence of execution.

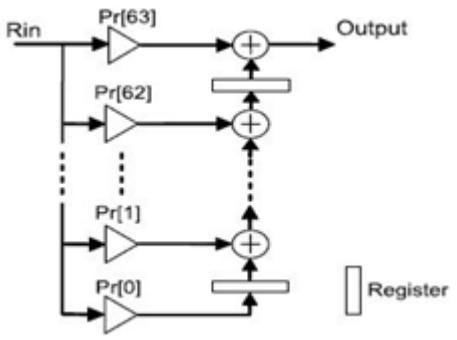


Fig 2(a) Transpose direct form of correlator

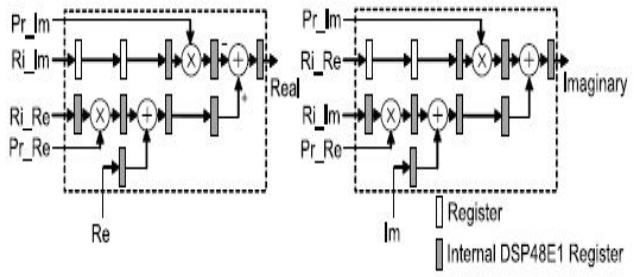


Fig 2(b) Pipeline structure for multiply-add

4.1 Design of multiplierless correlators:

The multiplier less correlators are represent the coefficients and round them in the form of summed powers of 2. Hence, a shift-and-add is performed instead of multiplying by coefficients. It is expected that multiplierless correlation is more efficient, but with embedded hard multipliers in modern FPGAs, it is unclear whether they should still be considered favorable. To compare the cost and performance and evaluate against multiplier-based correlators The multiplierless correlators is shown in Fig. 3.

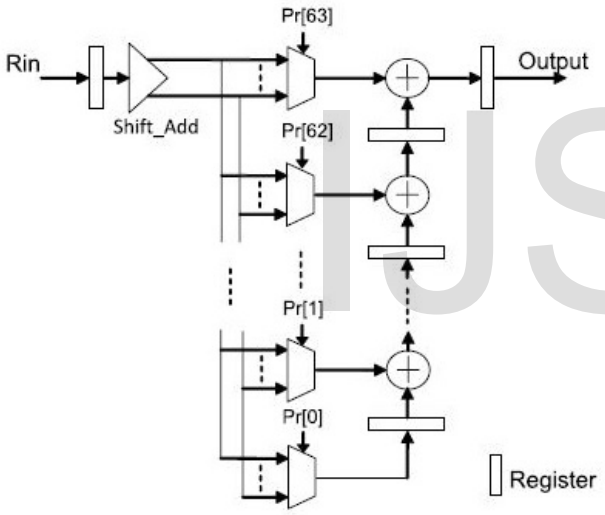


Fig .3. Multiplierless correlators

Using an multipliers to multiply input samples by coefficients, the Shift_Add block and multiplexers are used to perform the equivalent operation without an actual multiplication. But the Shift_Add block, multiplexers, and value of Pr[n] are different depending upon the quantized coefficient set being used. The Shift_Add block performs shift and add on the received samples according to the degree of quantization that is applied. The multiplexers are used for corresponding values from Shift_Add to accumulate in order to generate the correlator output. These are based on the expressed coefficients Pr[n] that are precomputed on the basis of quantizing the 64 preamble samples. The Pr[n] values are constants, after synthesizing the design, the multiplexer is optimized as hard-wired logic, and the preamble cannot be changed. To support different OFDM preambles and a real multiplexer used instead of hard-wired logic. This results in increased resource utilization but provides a more flexible solution.

4.2 Radix-2 FFT:

The existing system of multiplierless correlator is basically for an the radix-2 FFT based design. The computation of the N = 2 point DFT by the divide-and conquer approach. We split the N-point data sequence into two N/2-point data sequences f1(n) and f2(n), corresponding to the even-numbered and odd-numbered samples of x(n) respectively, that is,

$$f_1(n) = x(2n)$$
$$f_2(n) = x(2n+1), \qquad n = 0,1,\ldots,\frac{N}{2}-1$$

Thus f1(n) and f2(n) are obtained by decimating x(n) by a factor of 2, and hence the resulting FFT algorithm is called a decimation in-time algorithm. Now the N-point DFT can be expressed in terms of the DFT's of the decimated sequences:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}, \qquad k = 0,1,\ldots,N-1$$
$$= \sum_{n\ \text{even}} x(n) W_N^{kn} + \sum_{n\ \text{odd}} x(n) W_N^{kn}$$
$$= \sum_{m=0}^{(N/2)-1} x(2m) W_N^{2mk} + \sum_{m=0}^{(N/2)-1} x(2m+1) W_N^{k(2m+1)}$$

We observe that the direct computation of F1(k) requires (N/2)2 complex multiplications. The same applies to the computation of F2(k). Furthermore, there are N/2 additional complex multiplications required to compute WNkF2(k). Hence the computation of X(k) requires 2(N/2)2 + N/2 = N 2/2 + N/2 complex multiplications. This first step results in a reduction of the number of multiplications from N 2 to N 2/2 + N/2, which is about a factor of 2 for N large.

4.3 Mixed Radix FFT:

The split-radix FFT (SRFFT) algorithms exploit this idea by using both a radix-2 and a radix-4 decomposition in the same FFT algorithm. First, we recall that in the radix-2 decimation-in-frequency FFT algorithm, the even-numbered samples of the N-point DFT are given as,

$$X(2k) = \sum_{n=0}^{N/2-1} \left[x(n) + x\left(n+\frac{N}{2}\right) \right] W_{N/2}^{n}, \qquad k = 0,1,\ldots,\frac{N}{2}-1$$

5 SIMULATION RESULTS

5.1 OFDM Transmitter:

OFDM Transmitter is to be designed for an the multiplierless structure for replacing of multipliers in shift_adder and multiplexer. Without affecting of an the physical parameters and it's values are not changed in OFDM system. To achieve this output with the help of model sim and Xilinx simulator. The OFDM Transmitter

which has to be transmitted as an encryption scheme. The encryption scheme which involves BPSK, Cyclic prefix, Serial to parallel converter and parallel to serial conversions.

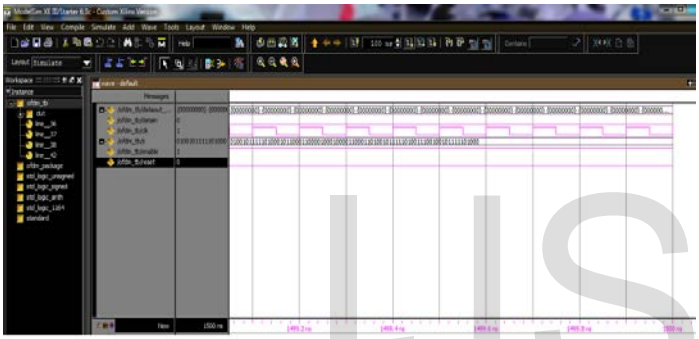
5.1.1 BPSK(Binary Phase Shift Keying):

BPSK is an the Encoding scheme. Which it contains both modulation and de-modulation scheme. Consider a sinusoidal carrier. The information about the bit stream is contained in the changes of phase of the transmitted signal. A synchronous demodulator would be sensitive to these phase reversals.

5.1.2 Cyclic prefix:

The cyclic prefix for x[n] is defined as {x[N − μ], . . . , x[N −1]}: it consists of the last μ values of the x[n] sequence. For each input sequence of length N, these last μ samples are appended to the beginning of the sequence.

5.1.3 OFDM Transmitter Serial to parallel converter output(010010):



This output which shows an serial to parallel conversion process at transmitter stage in the modelsim output at the input of sequence 010010.

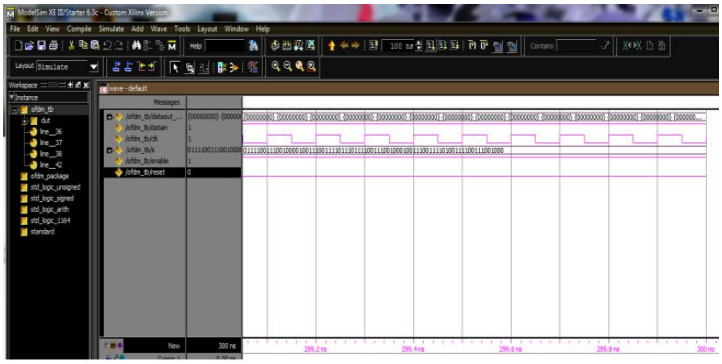
5.2 OFDM Receiver:

The OFDM receiver is an decryption/demodulator scheme. Receiver which involves inverse cyclic prefix, parallel to serial and Viterbi decoder.

5.2.1 Viterbi Decoder:

They are user parameterized to implement any number of standard decoders, or to quickly realize a custom application.

5.2.2 OFDM Receiver Parallel to Serial output : (011110)



Receiver output which shows an the conversion of parallel to serial output to recover an original information for sequence of 011110.

5.2.3 MB-OFDM Device summary:

TABLE 1
COMPARISON OF RADIX-2 AND MIXED RADIX FFT

	Area	Used	Available	Percentage
Radix-2 FFT	No of shift registers	2074	21,504	9%
Mixedradix FFT	No of shift registers	714	21,504	3%

Table 1 which shows an the comparison of area reduction achievement in MB-OFDM system.

6 CONCLUSION

The OFDM system is an more important for wired, wireless and optical communication. It gives an more synchronization accuracy for an communication field. OFDM has been implementing in less computation time.

6.1 Existing system:

The IEEE 802.16 OFDM synchronization can achieved the low power scheme is proposed. This scheme of design is consider for an multiplierless correlator. The multiplier based structure is require an more power and cost high. So, the proposed system has an replacement of multiplier to multiplierless structure to achieve the same output as an the multiplier based structure. The multiplierless structure which involves an shift_add and multiplier to achieve an low cost and low power device.

6.3 Future work:

This project is useful for achieve an more synchronization accuracy in communication field. The existing system which consists for radix-2 FFT and using in single carrier system

only. The proposed method is to develop a new Radix Based FFT Algorithm for the analysis of Multiband OFDM and their FPGA parameters calculation, in order to reduce the complexity for the efficient operation of MB-OFDM. Multi-Band orthogonal frequency division multiplexing reduces area than normal orthogonal frequency division multiplexing technique in Virtex-4 FPGA devices. Therefore the area reduction of MB-OFDM in mixed radix FFT has been achieved at 6% less compare over the existing system.In Table1 which gives an the exact output result for an the acheievement of area reduction is proved.

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BIOGRAPHIES

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Author's Photo

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